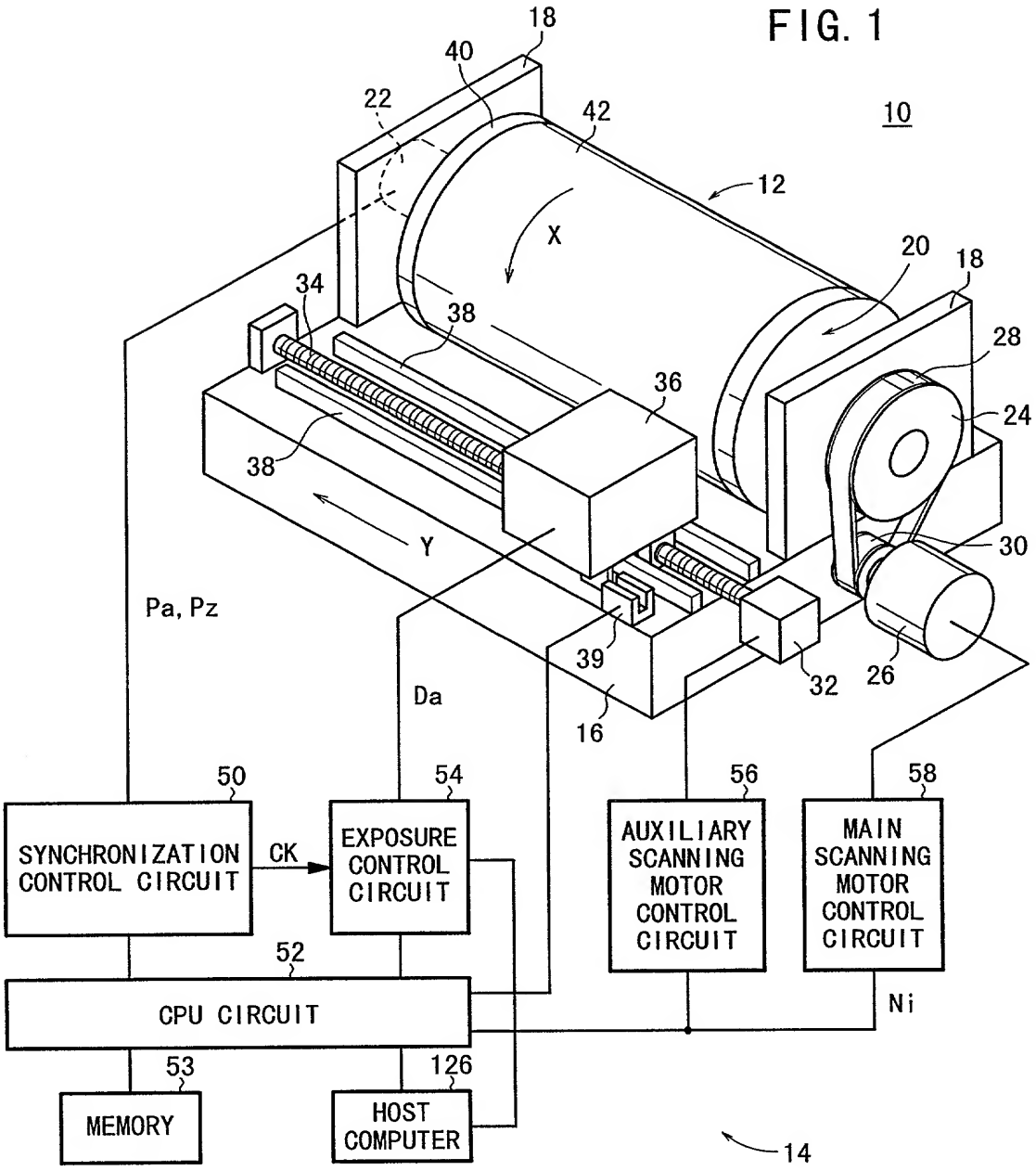
2002-0003-001

FIG. 1



09847270 "01/16/02

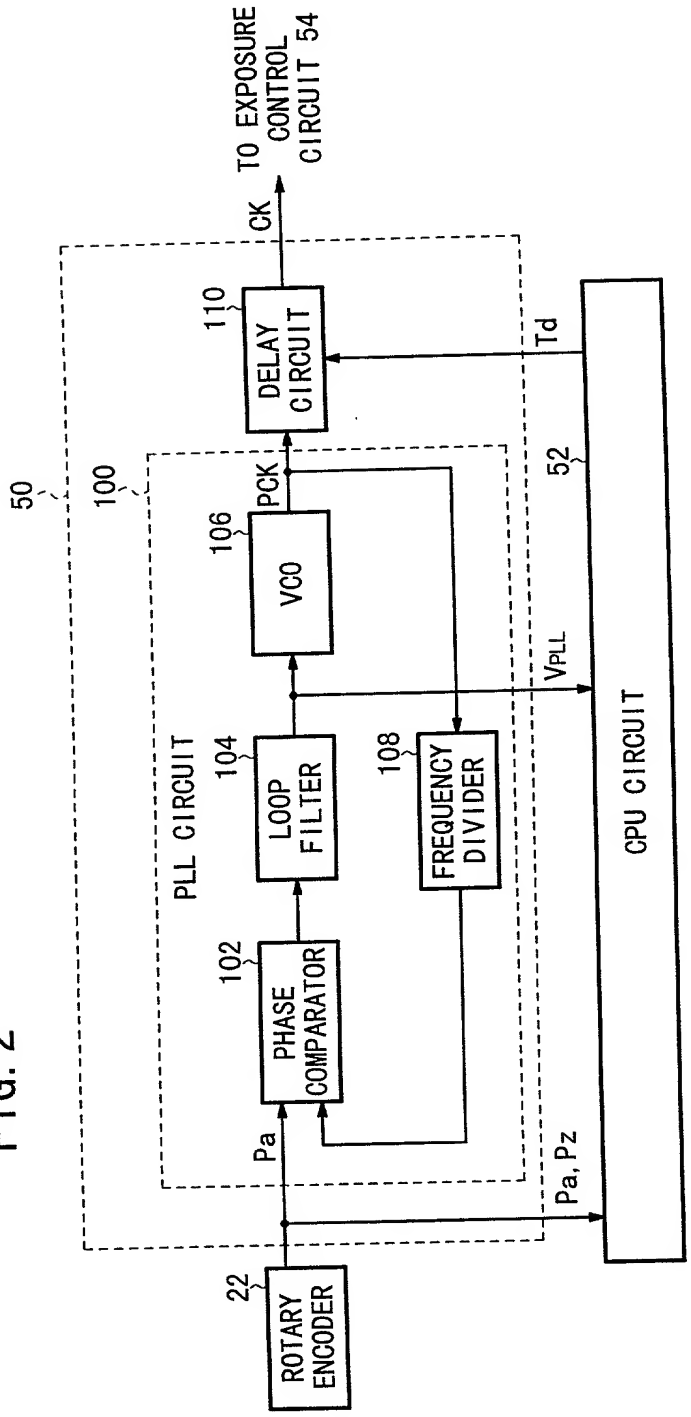


FIG. 2

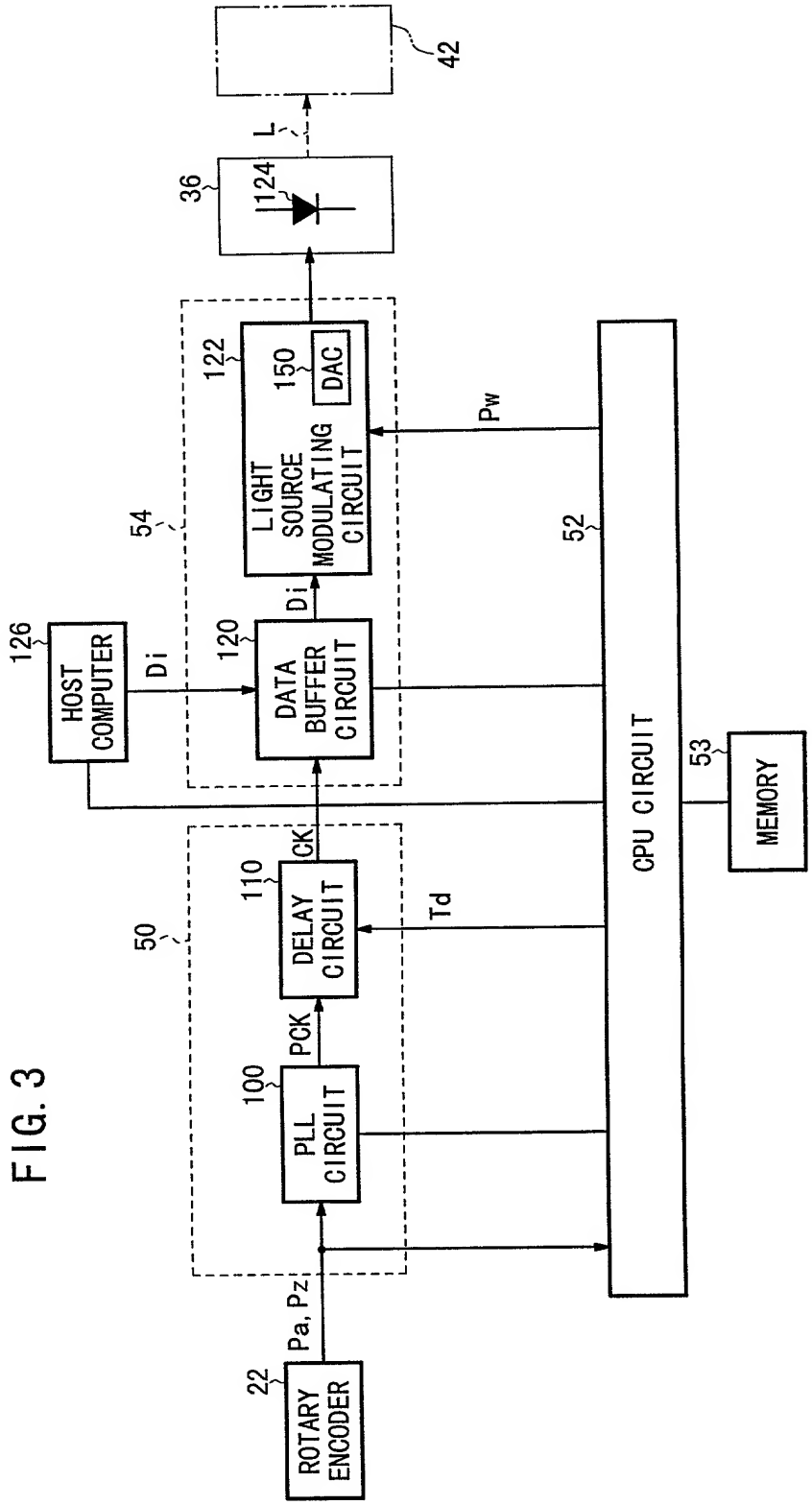

42
L
36
124
122
150
DAC
LIGHT SOURCE MODULATING CIRCUIT
Pw
54
52
126
HOST COMPUTER
Di
120
DATA BUFFER CIRCUIT
Di
CPU CIRCUIT
53
MEMORY
CK
110
DELAY CIRCUIT
Td
50
PCK
100
PLL CIRCUIT
Pa, Pz
22
ROTARY ENCODER

FIG. 3

FIG. 4A

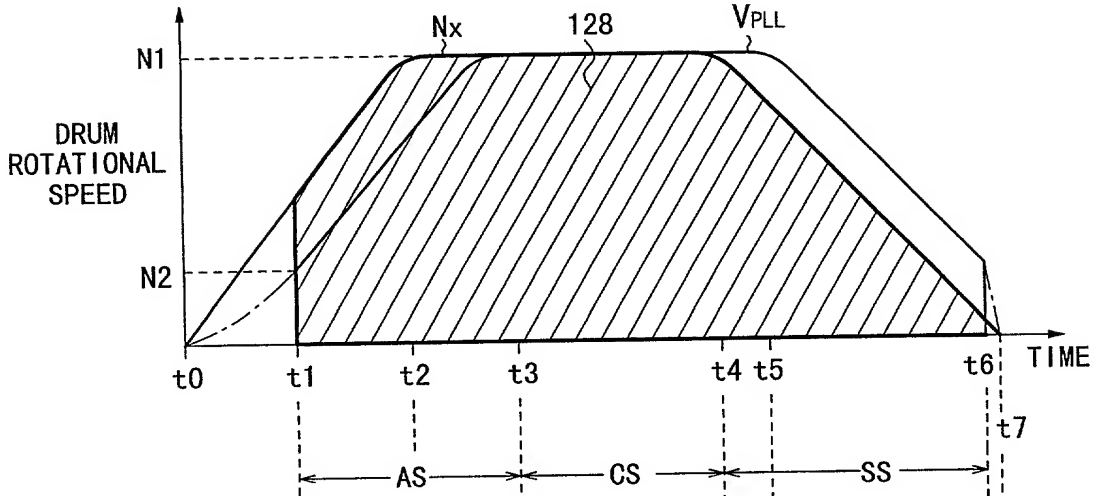


FIG. 4B

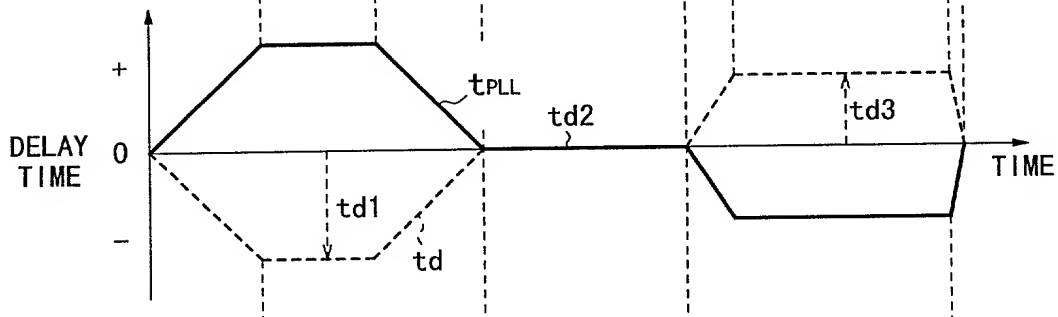


FIG. 4C

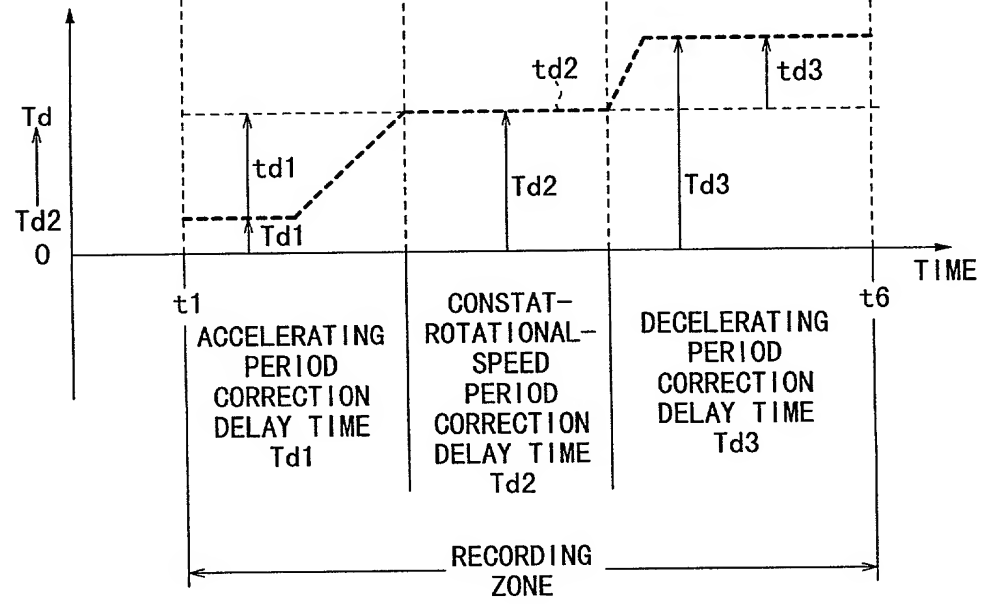
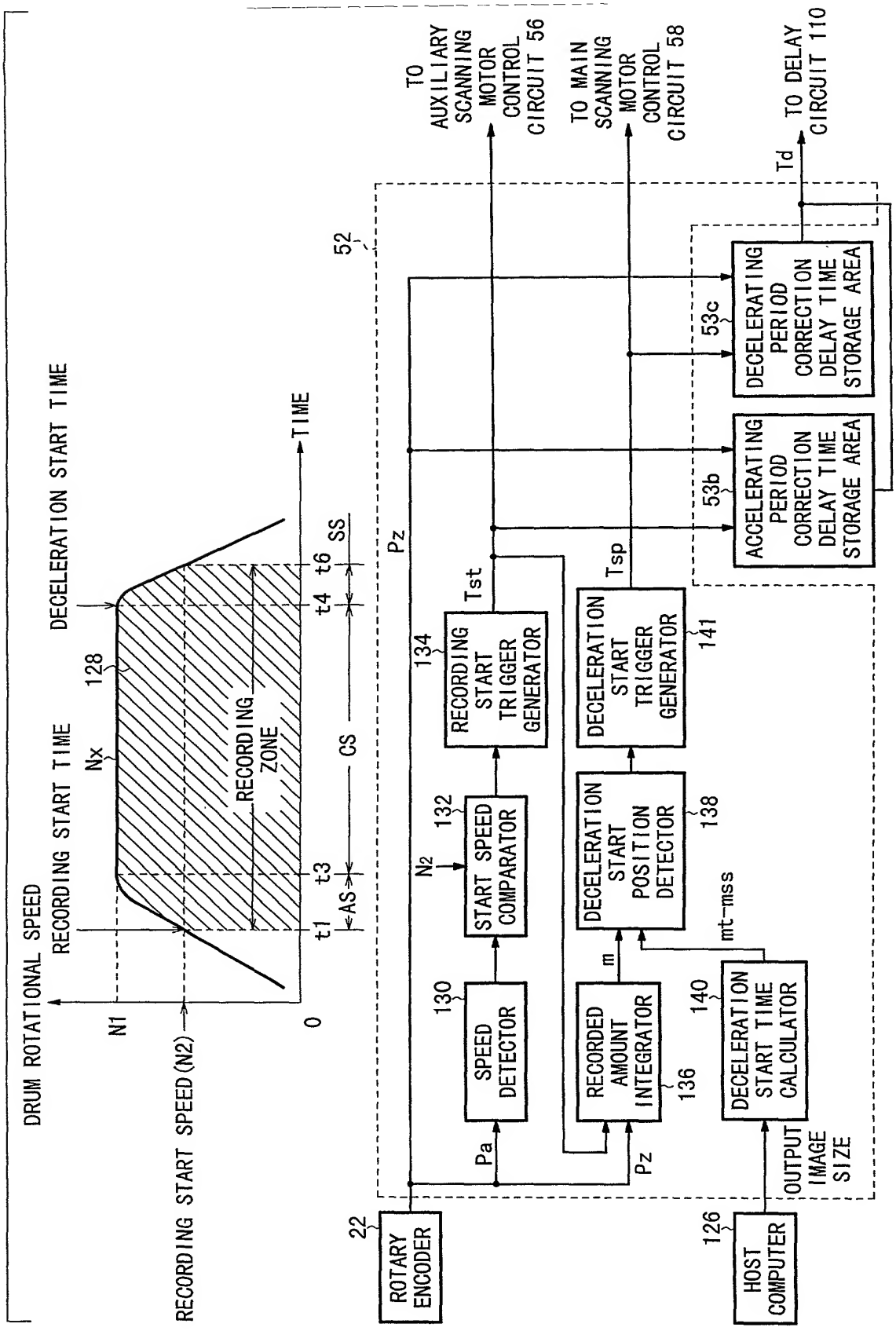


FIG. 5

53

STORAGE AREA		ADDRESS	DATA
53a	BASIC DELAY TIME DATA td	ADa | ADb	td1 | td2 | td3
53b	ACCELERATING PERIOD CORRECTION DELAY TIME	ADc | ADd	Td1 | Td2
53c	DECELERATING PERIOD CORRECTION DELAY TIME	ADe | ADf	Td2 | Td3
53d	ACCELERATING PERIOD LASER OUTPUT	ADg | ADh	Pwa | Pwc
53e	DECELERATING PERIOD LASER OUTPUT	ADi | ADj	Pwc | Pws
		⋮	

FIG. 6


DRUM ROTATIONAL SPEED
RECORDING START TIME
DECELERATION START TIME
TIME
Nx
128
N1
RECORDING START SPEED(N2)
RECORDING ZONE
0
t1
t3
AS
CS
t4
t6
SS
52
TO AUXILIARY SCANNING MOTOR CONTROL CIRCUIT 56
TO MAIN SCANNING MOTOR CONTROL CIRCUIT 58
TO DELAY CIRCUIT 110
Td
Pz
Tst
Tsp
134
RECORDING START TRIGGER GENERATOR
141
DECELERATION START TRIGGER GENERATOR
53c
DECELERATING PERIOD CORRECTION DELAY TIME STORAGE AREA
53b
ACCELERATING PERIOD CORRECTION DELAY TIME STORAGE AREA
N2
132
START SPEED COMPARATOR
DECELERATION START POSITION DETECTOR
138
m
mt-mss
130
SPEED DETECTOR
RECORDED AMOUNT INTEGRATOR
136
140
DECELERATION START TIME CALCULATOR
Pa
Pz
OUTPUT IMAGE SIZE
22
ROTARY ENCODER
126
HOST COMPUTER

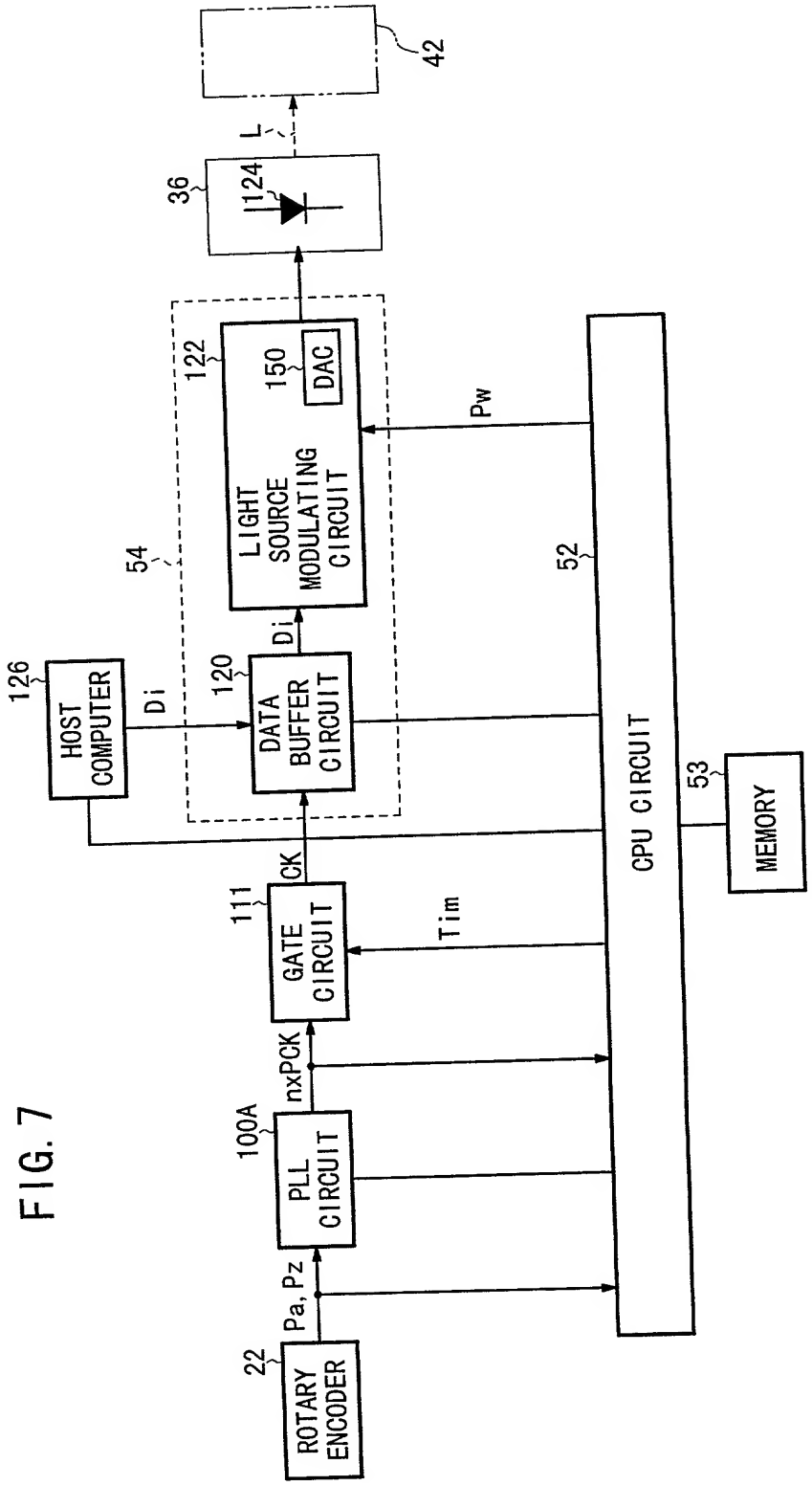

42
L
36
124
122
150
DAC
LIGHT SOURCE MODULATING CIRCUIT
Pw
54
52
126
HOST COMPUTER
Di
120
DATA BUFFER CIRCUIT
Di
CPU CIRCUIT
53
MEMORY
CK
111
GATE CIRCUIT
Tim
nxPCK
100A
PLL CIRCUIT
Pa, Pz
22
ROTARY ENCODER

FIG. 7

20070702.020404.0015

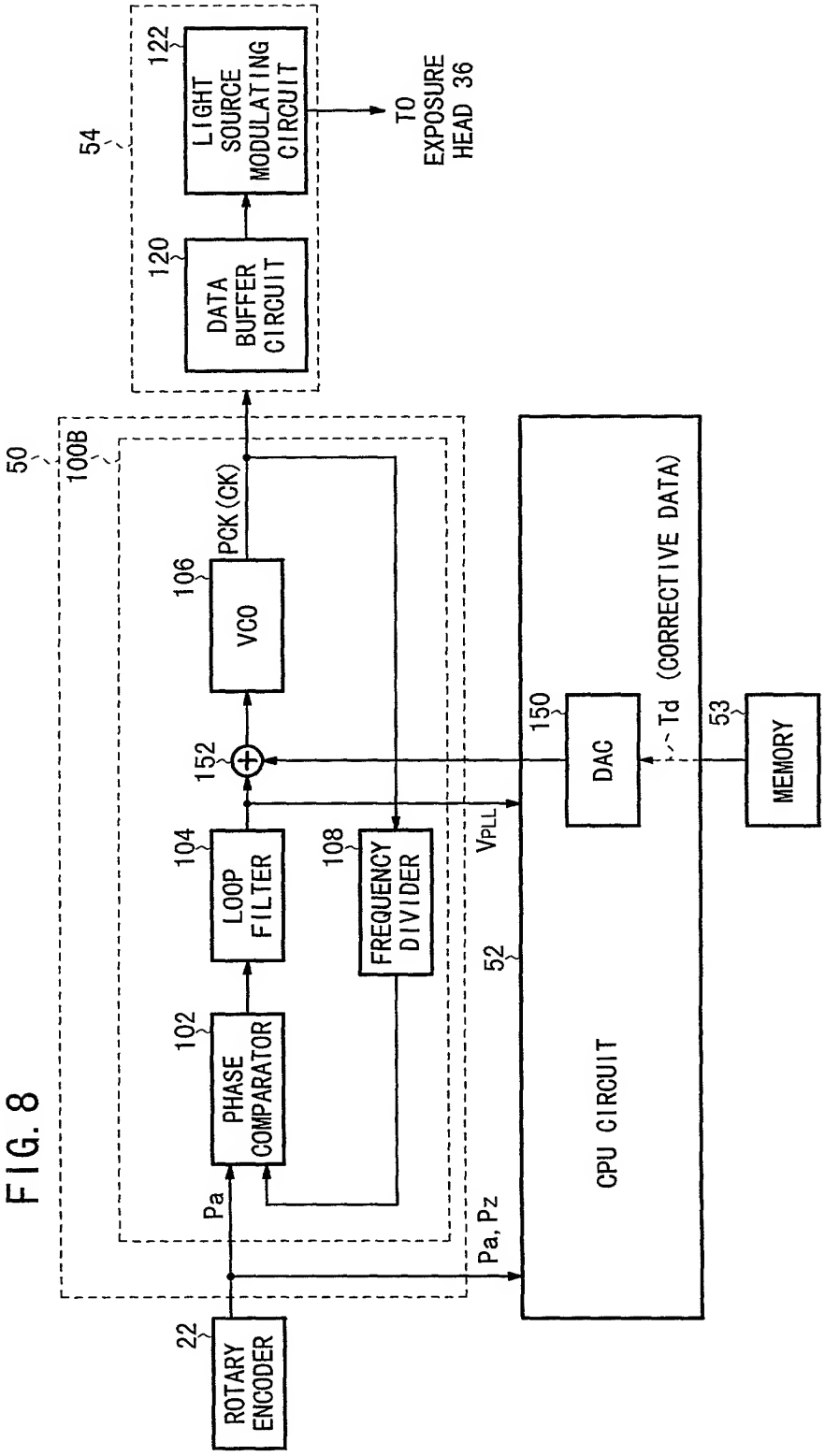


FIG. 8

FIG. 9A

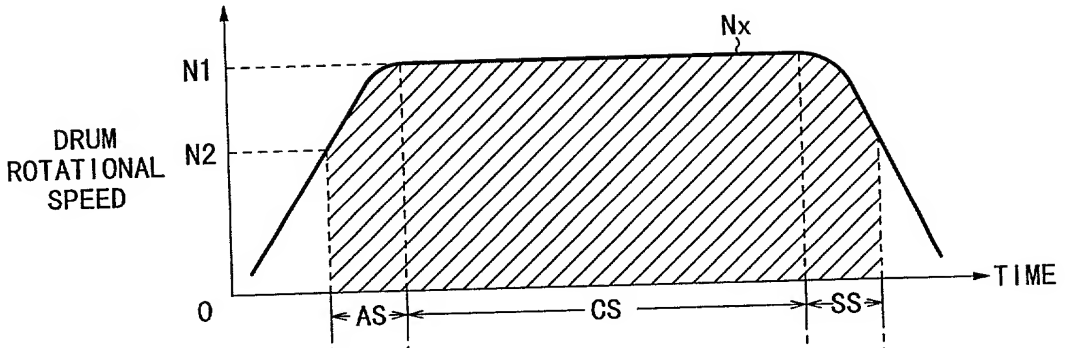

Nx
N1
N2
DRUM
ROTATIONAL
SPEED
TIME
0
AS
CS
SS

FIG. 9B

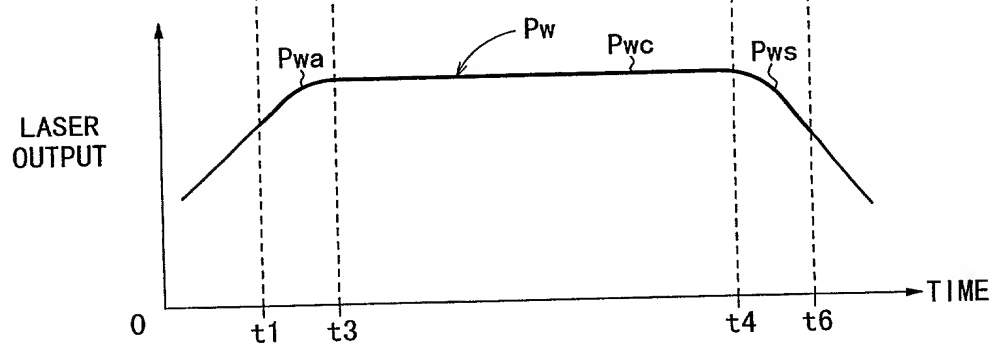

Pw
Pwa
Pwc
Pws
LASER
OUTPUT
TIME
0
t1
t3
t4
t6

FIG. 10

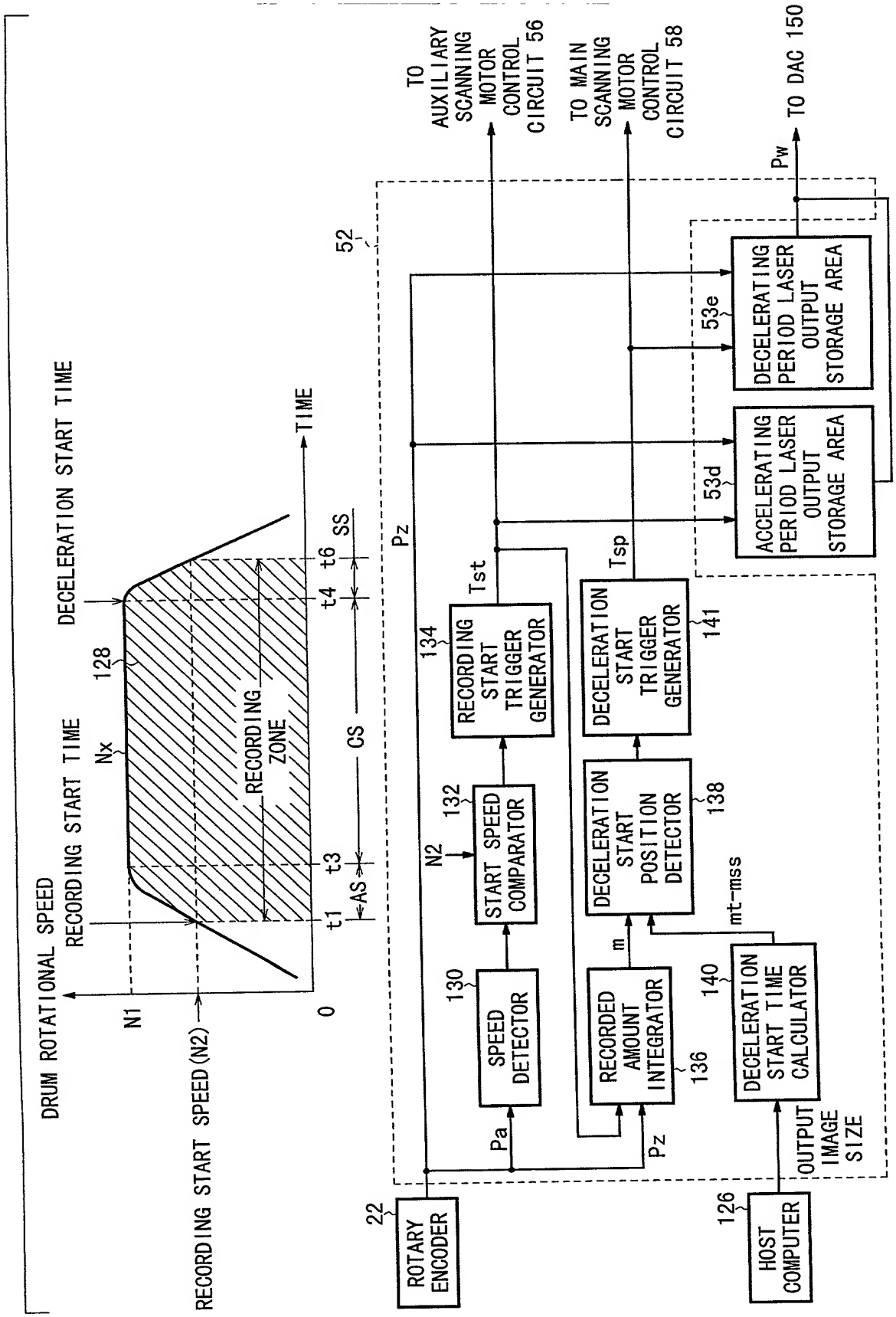

DRUM ROTATIONAL SPEED
RECORDING START TIME
DECELERATION START TIME
TIME
Nx
128
N1
RECORDING START SPEED (N2)
RECORDING ZONE
0
t1
t3
t4
t6
AS
CS
SS
52
TO AUXILIARY SCANNING MOTOR CONTROL CIRCUIT 56
TO MAIN SCANNING MOTOR CONTROL CIRCUIT 58
Pw
TO DAC 150
Pz
Tst
Tsp
134
RECORDING START TRIGGER GENERATOR
141
DECELERATION START TRIGGER GENERATOR
53e
DECELERATING PERIOD LASER OUTPUT STORAGE AREA
53d
ACCELERATING PERIOD LASER OUTPUT STORAGE AREA
N2
132
START SPEED COMPARATOR
138
DECELERATION START POSITION DETECTOR
mt-mss
m
130
SPEED DETECTOR
RECORDED AMOUNT INTEGRATOR
136
140
DECELERATION START TIME CALCULATOR
Pa
Pz
OUTPUT IMAGE SIZE
22
ROTARY ENCODER
126
HOST COMPUTER

FIG. 11

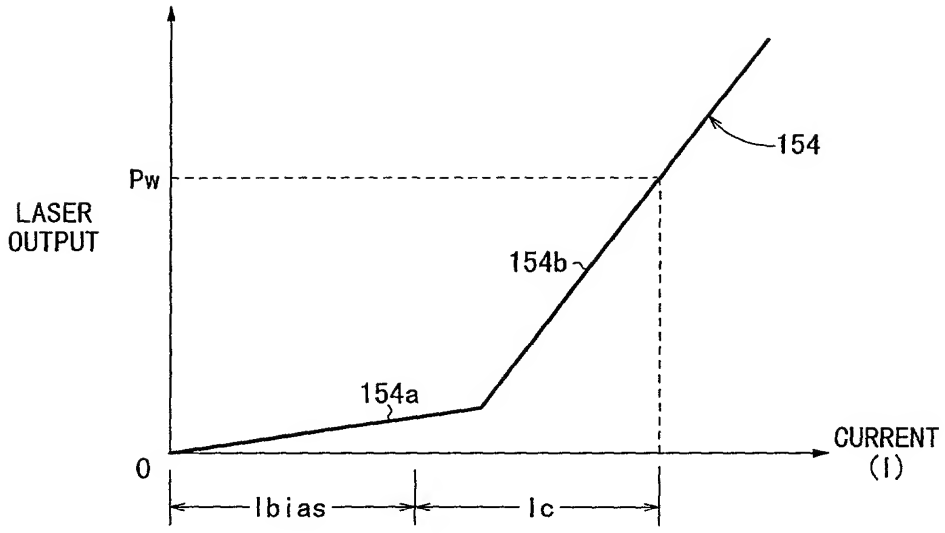


FIG. 12

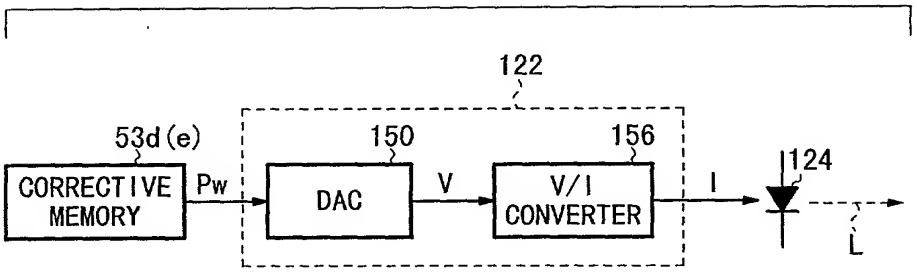
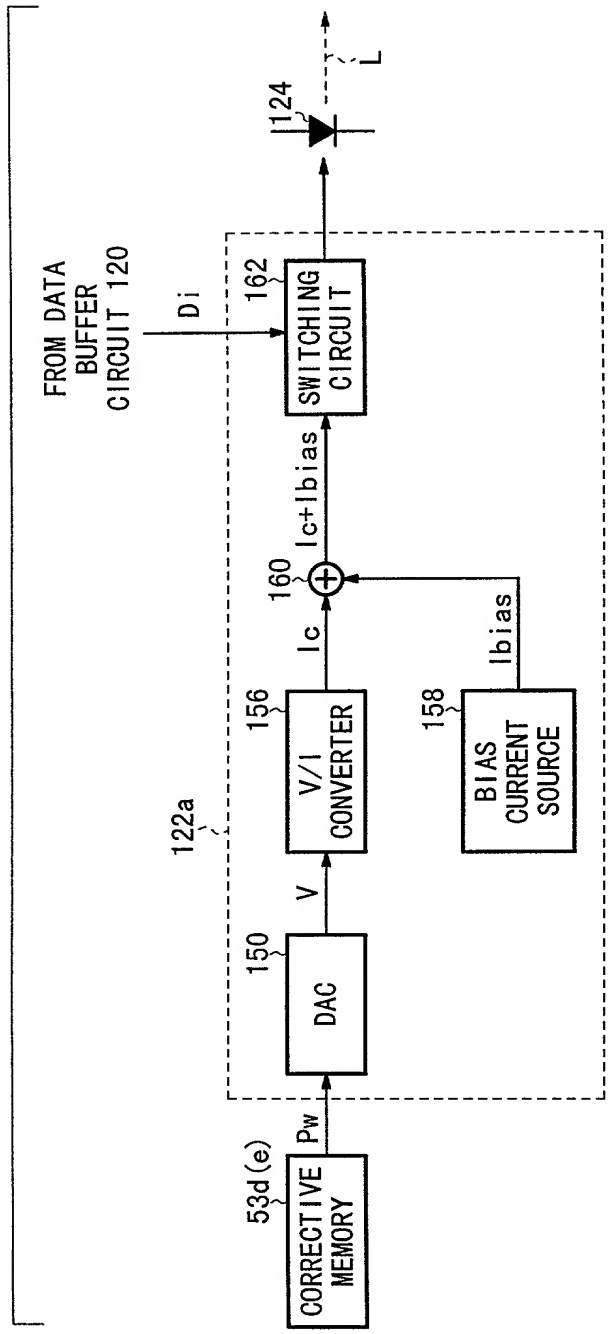

122
53d(e)
150
156
124
CORRECTIVE MEMORY
Pw
DAC
V
V/I CONVERTER
I
L

FIG. 13


FROM DATA BUFFER CIRCUIT 120
Di
162
SWITCHING CIRCUIT
124
L
Ic+Ibias
160
Ic
Ibias
156
V/I CONVERTER
158
BIAS CURRENT SOURCE
122a
150
DAC
V
53d(e)
CORRECTIVE MEMORY
Pw

apparent" 6/26/04 4:00:04 PM

FIG. 14

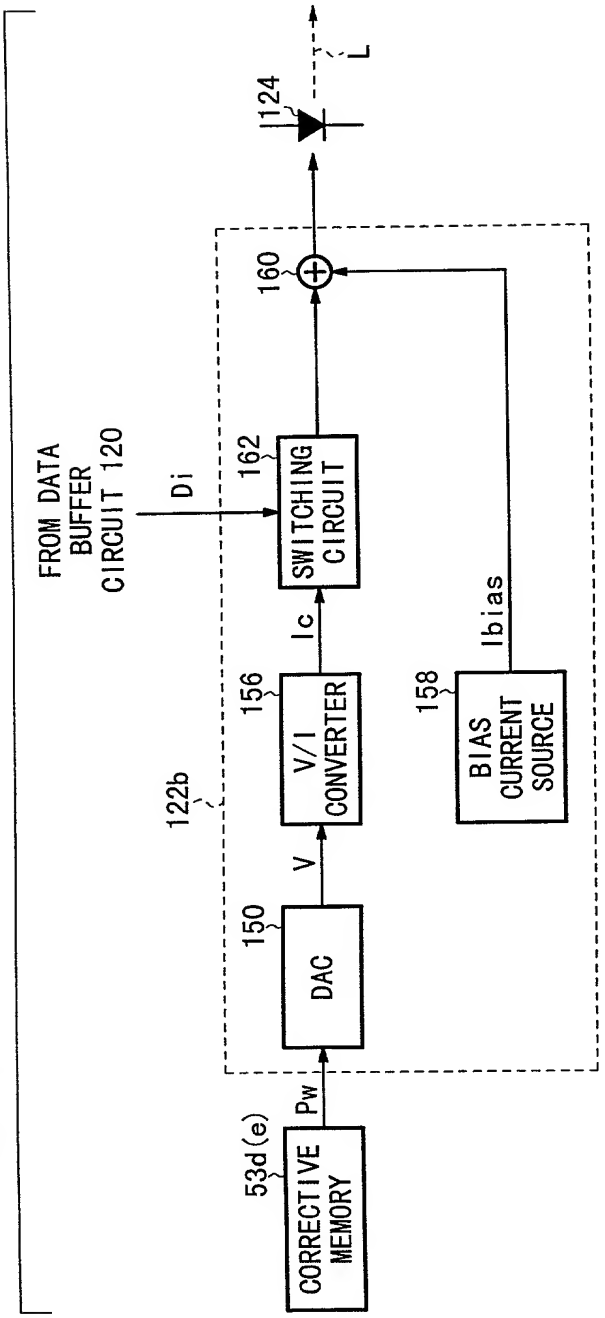
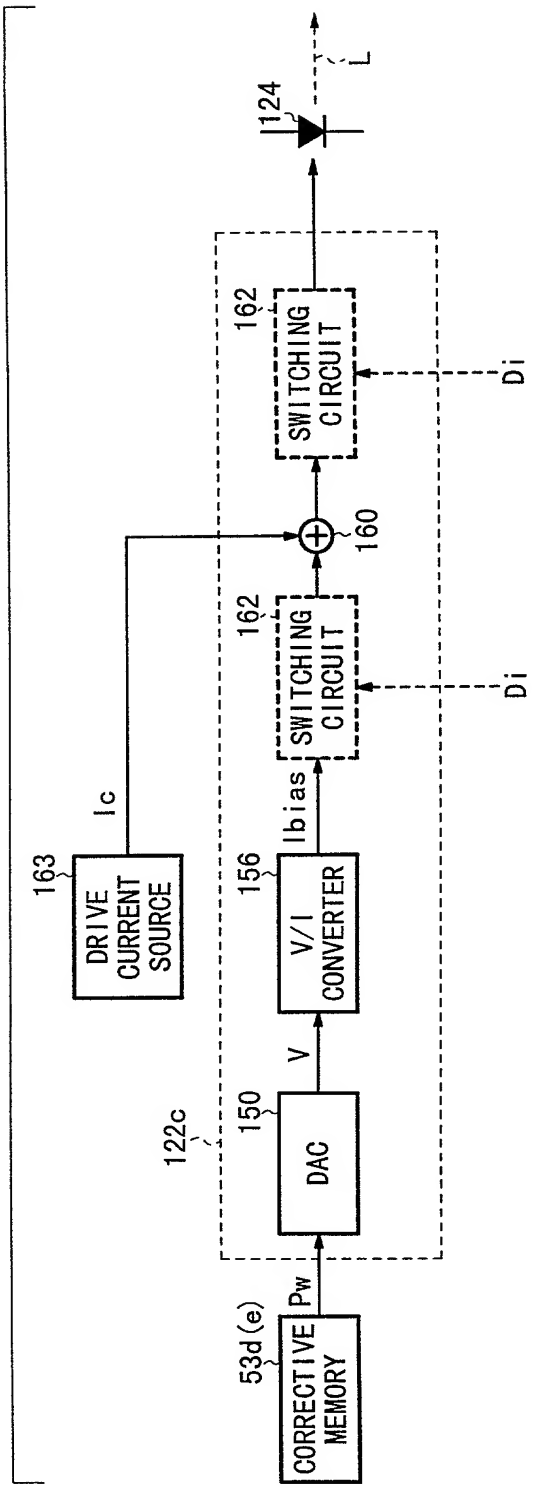


FIG. 15


124
L
162
SWITCHING CIRCUIT
Di
160
162
SWITCHING CIRCUIT
Di
Ic
163
DRIVE CURRENT SOURCE
156
V/I CONVERTER
Ibias
122c
150
DAC
V
53d(e)
CORRECTIVE MEMORY
Pw

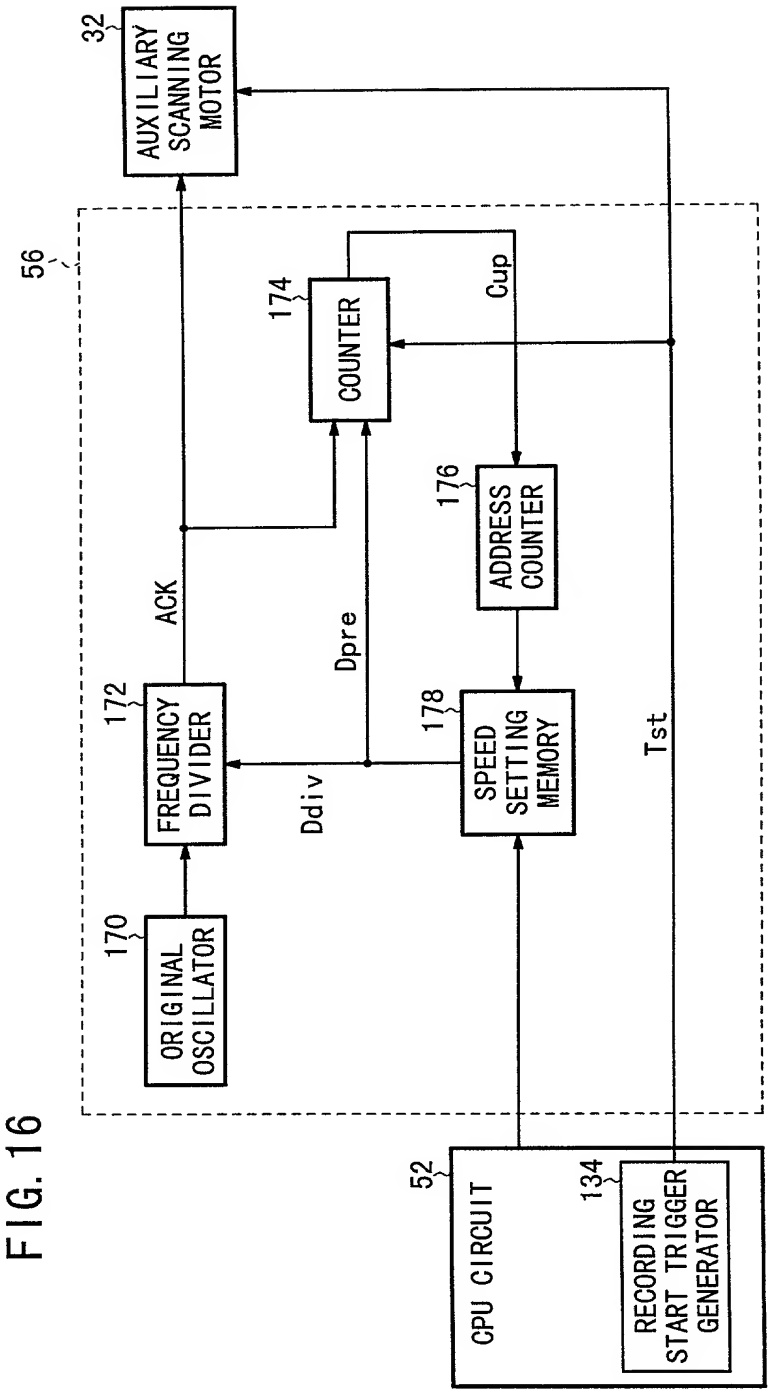

32
AUXILIARY SCANNING MOTOR
56
174
COUNTER
Cup
176
ADDRESS COUNTER
ACK
Dpre
172
FREQUENCY DIVIDER
178
SPEED SETTING MEMORY
Tst
Ddiv
170
ORIGINAL OSCILLATOR
52
CPU CIRCUIT
134
RECORDING START TRIGGER GENERATOR

FIG. 16

FIG. 17

178

ADDRESS	FREQUENCY-DIVIDING RATIO (Ddiv)	PRESET VALUE (Dpre)	APPARATUS OPERATING STATUS
1	100	50	ACCELERATION STARTED
2	95	48	IN ACCELERATION
3	90	46	DITTO
4	85	44	DITTO
5	80	1000	AT CONSTANT SPEED
6	85	44	DECELERATION STARTED
7	90	46	IN DECELERATION
8	95	48	DITTO
9	100	50	DECELERATION ENDED

Sheet 17 of 22 Drawings

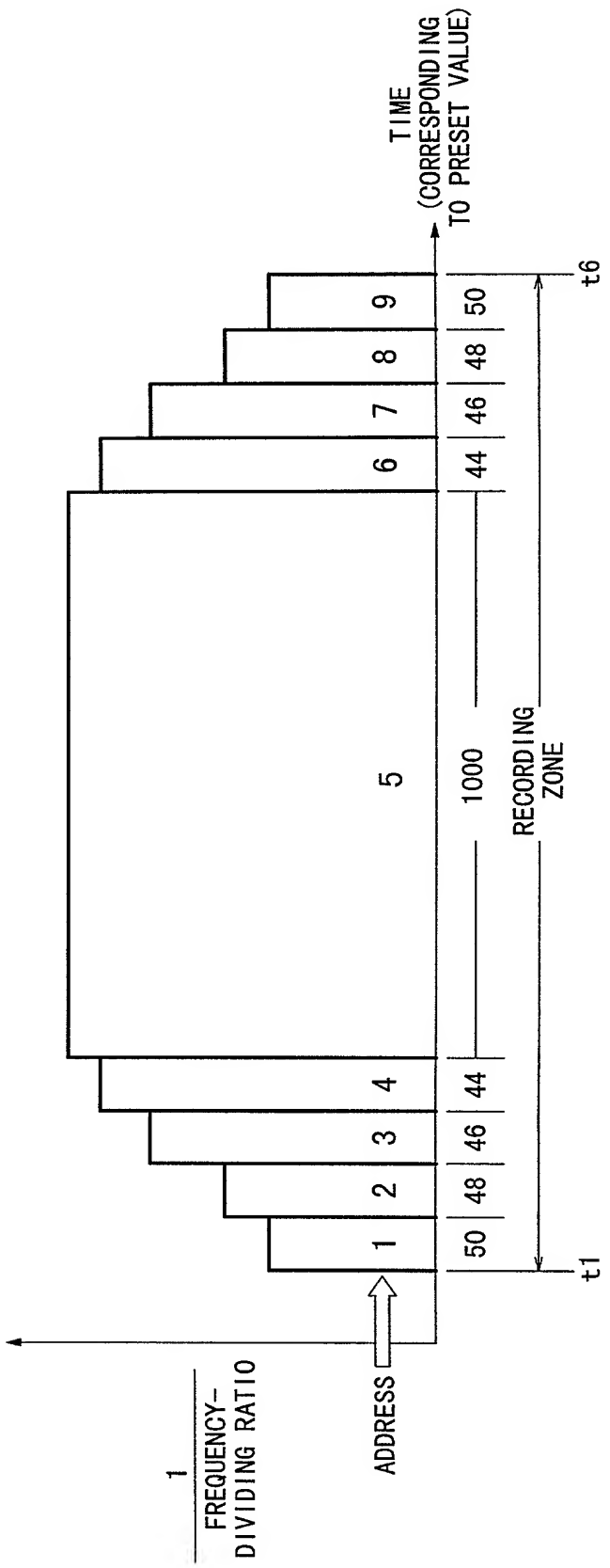

TIME
(CORRESPONDING
TO PRESET VALUE)
t6
t1
RECORDING
ZONE
1000
50
48
46
44
1
2
3
4
5
6
7
8
9
ADDRESS
1
FREQUENCY-
DIVIDING RATIO

FIG. 18

FIG. 19

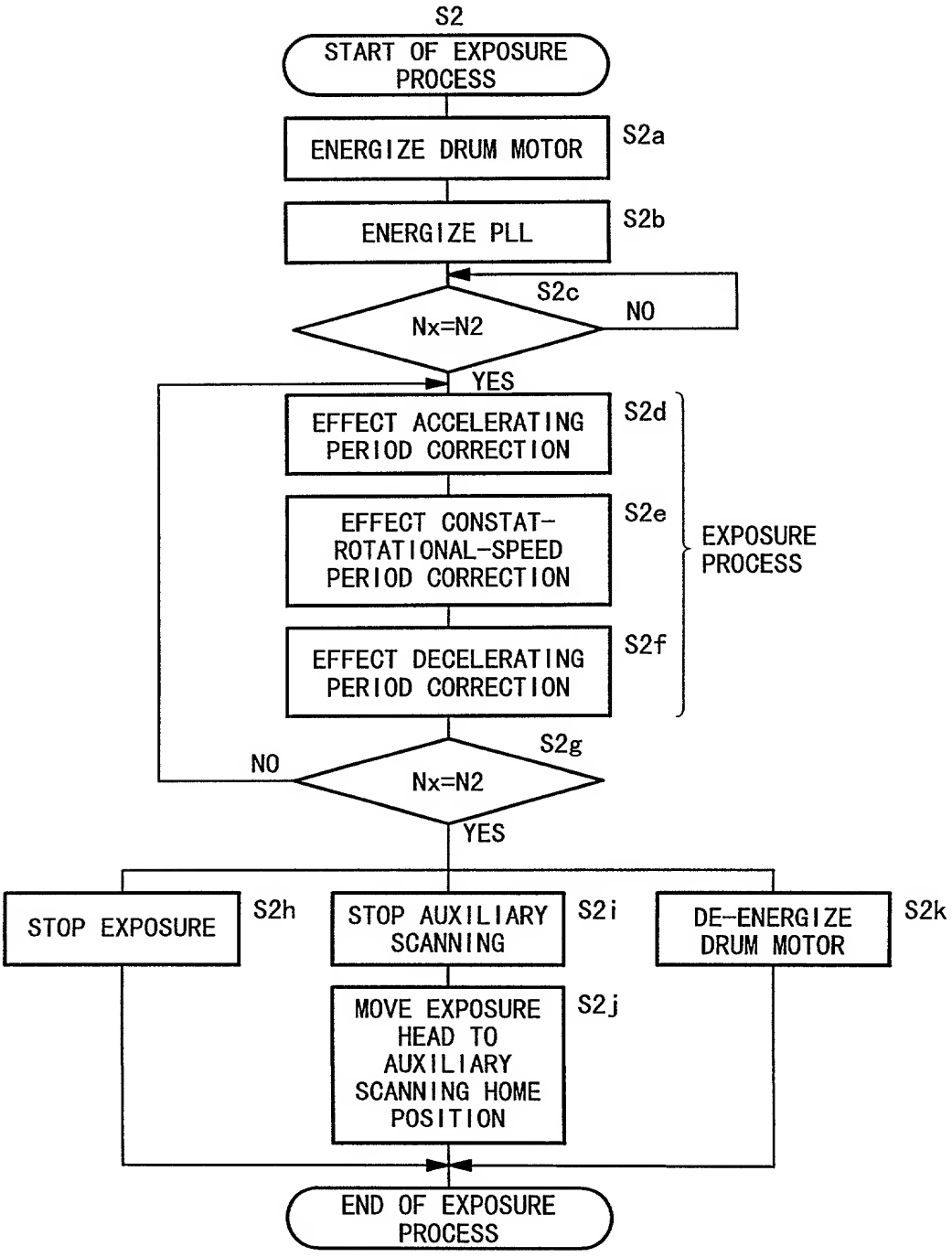

S2
START OF EXPOSURE PROCESS
ENERGIZE DRUM MOTOR
S2a
ENERGIZE PLL
S2b
S2c
Nx=N2
NO
YES
EFFECT ACCELERATING PERIOD CORRECTION
S2d
EFFECT CONSTAT-ROTATIONAL-SPEED PERIOD CORRECTION
S2e
EFFECT DECELERATING PERIOD CORRECTION
S2f
EXPOSURE PROCESS
S2g
NO
Nx=N2
YES
STOP EXPOSURE
S2h
STOP AUXILIARY SCANNING
S2i
DE-ENERGIZE DRUM MOTOR
S2k
MOVE EXPOSURE HEAD TO AUXILIARY SCANNING HOME POSITION
S2j
END OF EXPOSURE PROCESS

FIG. 20

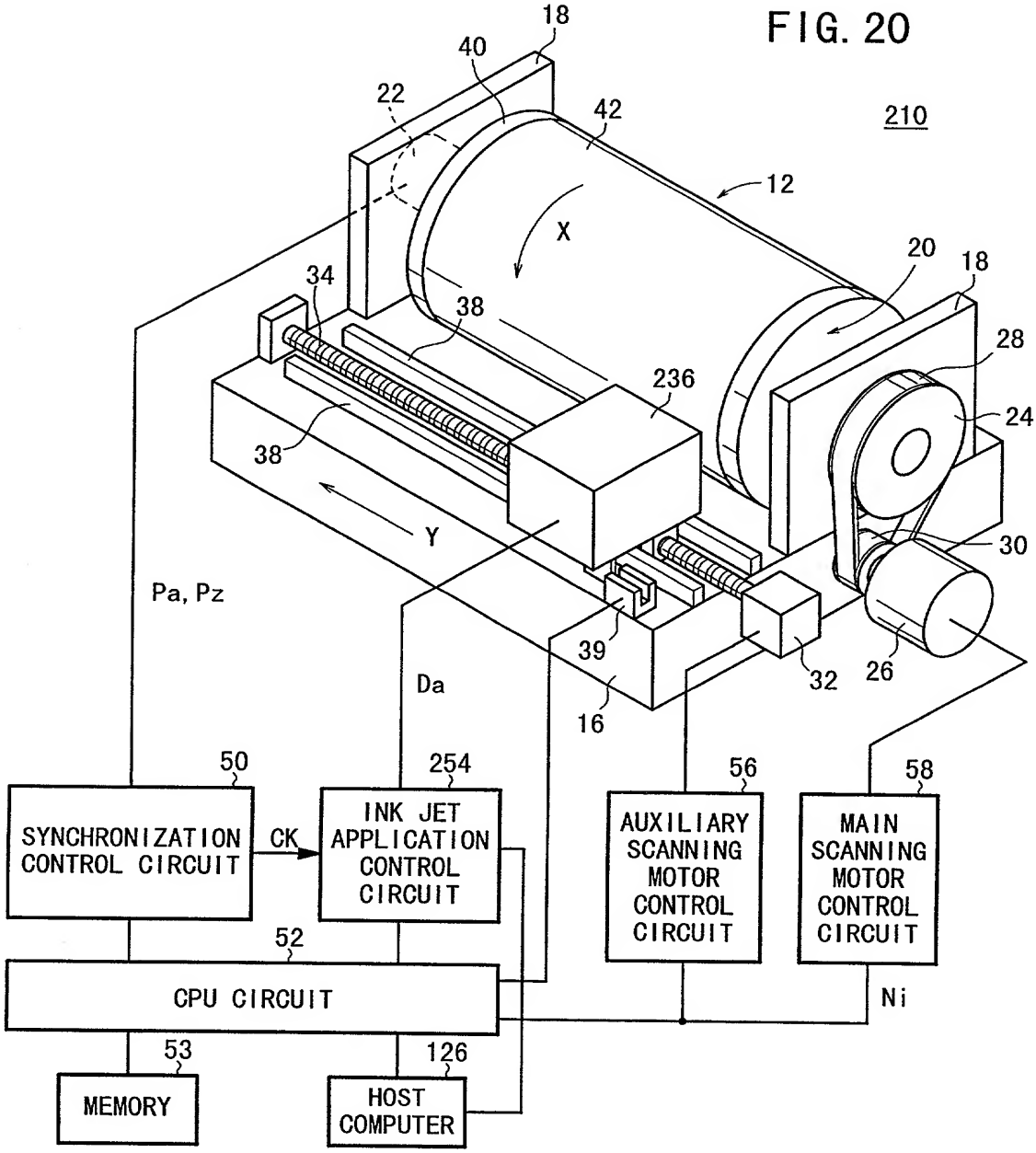

210
18
40
22
42
12
X
20
18
34
38
28
236
24
38
Y
30
Pa, Pz
39
32
26
Da
16
50
254
56
58
SYNCHRONIZATION CONTROL CIRCUIT
CK
INK JET APPLICATION CONTROL CIRCUIT
AUXILIARY SCANNING MOTOR CONTROL CIRCUIT
MAIN SCANNING MOTOR CONTROL CIRCUIT
52
CPU CIRCUIT
Ni
53
126
MEMORY
HOST COMPUTER

FIG. 21
PRIOR ART

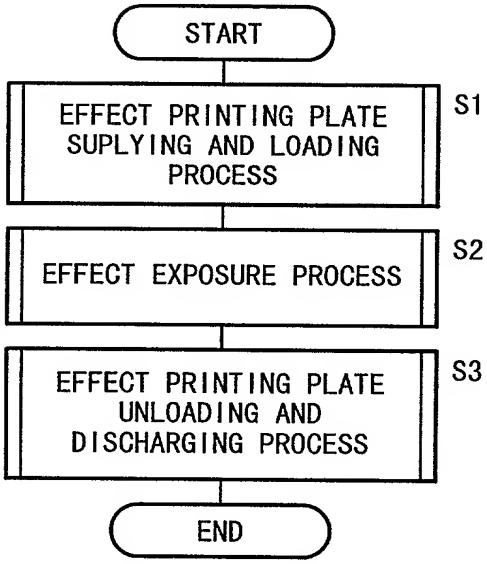


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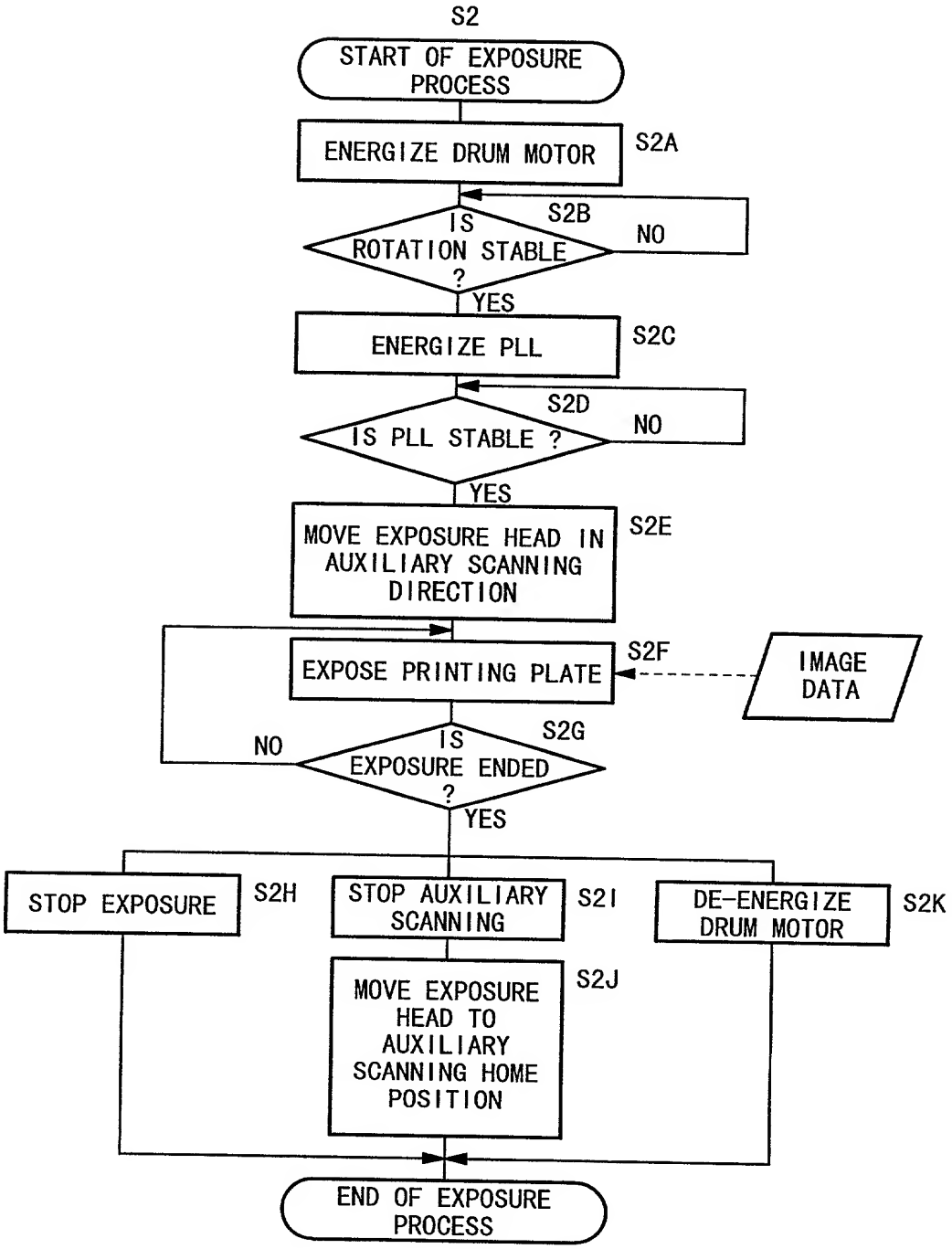
FIG. 22
PRIOR ART



US 6,606,098 B2